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23 ~~41~~. The input buffer circuit according to claim 20 ~~38~~, wherein the control circuit enables the differential amplifier circuit and the first circuit and disables the second circuit when the first and second input signals have amplitudes smaller than a predetermined voltage.

24 ~~42~~. The input buffer circuit according to claim 20 ~~38~~, wherein the control circuit disables the differential amplifier circuit and the first circuit and enables the second circuit when the first and second input signals have amplitudes greater than a predetermined voltage.

REMARKS

The Office Action dated October 19, 2001 has been received and carefully noted. The preceding amendments and the following remarks are submitted as a full and complete response thereto. Claims 11-16 have been canceled without prejudice or disclaimer. Claims 19-42 have been added. New claims 19-42 are supported by the specification at page 11, line 15 to page 13, line 31. No new matter has been added. Accordingly, Claims 19-42 are pending in this application and are submitted for consideration.

The drawings were objected to for several informalities. In particular, it was asserted that Fig. 6 does not have text labels on its black boxes, and that the two switches in Fig. 6 have not been provided with a reference numeral. Accordingly, attached hereto is a corrected Fig. 6 with text labels for each black box, and labeling the

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switches SW1 and SW2. The specification is also amended to include a description of switches SW1 and SW2. The drawings were also objected to because Fig. 6 includes a transfer circuit 4 that is a symbol of a tri-state inverter. The reference numeral has been amended from "4" to --4A--. Accordingly, Applicant requests that the objections to the drawings be withdrawn.

Claims 12 and 13 were rejected under 35 U.S.C. § 112, second paragraph, on the grounds that the recitations "small" in claim 12 and "full" in claim 13 were indefinite relative terms, and on the grounds that that the control circuit is independent with the first and second input signals of the input buffer circuit, and therefore that the amplitude of the first and second input signals does not affect "when" the control circuit enables or disables the differential amplifier, the first or the second tri-state inverter circuit.

Claims 11-16 have been canceled without prejudice or disclaimer. New claims 19-42 do not use the recitations "small" and "full", but instead use the recitations "amplitudes smaller than a predetermined voltage" and "amplitude greater than a predetermined voltage". Page 12, lines 18-30 of the specification, clearly describe that when the input signals IN and IN/ have small amplitudes, the control-signal output circuit 17 receives the input control circuit S-low. Accordingly, the control circuit enables the differential amplifier circuit and the first tri-state inverter circuit and disables the second tri-state inverter circuit. Similarly, at page 13, lines 7-19, it is clearly described that when the input signals IN and IN/ have full amplitudes, the control-signal output circuit 17 receives the input control signal S-high. In response, the differential amplifier circuit and the first tri-state inverter circuit are disabled and the second tri-state converter circuit is enabled. Accordingly, new claims do not include indefinite relative terms, and

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Applicant submits that claim 19-42 comply with all the requirements of 35 USC § 112 and requests that the rejections and objections be withdrawn.

Claims 11-13 were rejected under 35 USC § 102(b) as being anticipated by Roe et al. (U.S. Patent No. 5,929,655). Claim 14 was rejected under 35 USC § 103(a) as being unpatentable over Roe in view of Oldham (U.S. Patent No. 5,563,835). Claim 15 was rejected under 35 USC § 103(a) as being unpatentable over Roe in view of D'Souza (U.S. Patent No. 5,811,992). Claims 11-16 have been cancelled without prejudice or disclaimer. Applicant submits that new claims 19-42 recite subject matter which is not shown or suggested by any of the cited prior art.

Independent claim 19 recites an input buffer circuit that includes a differential amplifier circuit, a first and second circuit, and a control circuit. The differential amplifier circuit is disposed between a first power supply and a second power supply and is for receiving first and second input signals and for generating an amplified signal corresponding to a voltage difference between the first and second input signals. The first circuit is connected to the differential amplifier circuit and is for receiving the amplified signal from the differential amplifier circuit. The second circuit is disposed between the first power supply and the second power supply and is for receiving the first input signal. The control circuit is for selectively enabling the differential amplifier circuit and the second circuit in accordance with a control signal, wherein the control circuit isolates one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply.

Independent claim 22 recites an input buffer circuit that includes a differential amplifier circuit, a first and second circuit, and a control circuit. The differential amplifier

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circuit is for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals. The first circuit is connected to the differential amplifier circuit and is for receiving the amplified signal from the differential amplifier circuit. The second circuit is for receiving the first input signal. The control circuit is for selectively enabling the differential amplifier circuit and the second circuit in accordance with a control signal, wherein the control circuit enables the differential amplifier circuit and disables the second circuit when the first and second input signals have amplitudes smaller than a predetermined voltage.

Independent claim 25 recites an input buffer circuit that includes a differential amplifier circuit, a first and second circuit, and a control circuit. The differential amplifier circuit is for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals. The first circuit is connected to the differential amplifier circuit and is for receiving the amplified signal from the differential amplifier circuit. The second circuit is for receiving the first input signal. The control circuit is for selectively enabling the differential amplifier circuit and the second circuit in accordance with a control signal. The control circuit disables the differential amplifier circuit and enables the second circuit when the first and second input signals have amplitudes greater than a predetermined voltage.

Independent claim 28 recites an input buffer circuit that includes a differential amplifier circuit, a first and second circuit, and a control circuit. The differential amplifier circuit is for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals. The

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first circuit is connected to the differential amplifier circuit and is for receiving the amplified signal from the differential amplifier circuit. The second circuit is for receiving the first input signal. The control circuit is for selectively enabling the differential amplifier circuit and the first and second circuits in accordance with a control signal,. The differential amplifier circuit and the first circuit are enabled and the second circuit is disabled when the first and second input signals have amplitudes smaller than a predetermined voltage.

Independent claim 33 recites an input buffer circuit that includes a differential amplifier circuit, a first and second circuit, and a control circuit. The differential amplifier circuit is for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals. The first circuit is connected to the differential amplifier circuit and is for receiving the amplified signal from the differential amplifier circuit. The second circuit is for receiving the first input signal. The control circuit is connected to the differential amplifier circuit and the first and second circuits and is for selectively enabling the differential amplifier circuit and the first and second circuits in accordance with a control signal. The differential amplifier circuit and the first circuit are disabled and the second circuit is enabled when the first and second input signals have amplitudes greater than a predetermined voltage.

Independent claim 38 recites an input buffer circuit that includes a differential amplifier circuit, a first and second circuit, and a control circuit. The differential amplifier circuit is for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals. The

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first circuit is disposed between a first power supply and a second power supply, for receiving the amplified signal from the differential amplifier circuit. The second circuit is disposed between the first power supply and the second power supply and is for receiving the first input signal. The control circuit is connected to the differential amplifier circuit and the first and second circuits and is for selectively enabling the differential amplifier circuit and the first and second circuits in accordance with a control signal. The control circuit isolates one of the first circuit and the second circuit from the first power supply or the second power supply.

As a result of the claimed configurations, the present invention provides input buffers that have the following novel features: 1) a differential amplifier circuit (or the differential amplifier circuit and a first circuit) is enabled and a second circuit is disabled when first and second input signals have amplitudes smaller than a predetermined voltage (See claims 22 and 28); 2) a differential amplifier circuit (or the differential amplifier circuit and a first circuit) is disabled and a second circuit is enabled when first and second input signals have amplitudes greater than a predetermined voltage(See claims 25 and 33); or 3) a differential amplifier circuit and a second circuit (or a first circuit and the second circuit) are disposed between a first power supply and a second power supply and a control circuit isolates the differential amplifier circuit or the second circuit (or the first circuit or the second circuit) from the first power supply or the second power supply (See claims 19 and 38).

Roe is directed to a I/O circuit including a differential amplifier (210), a first output buffer (208), a second output buffer (202), and a control circuit (214). However, Roe does not describe or suggest selectively enabling/disabling the first and second output

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buffers according to amplitudes of input signals, as defined by the claimed invention. Furthermore, Roe does not describe or suggest a control circuit that controls to isolate the first output buffer or the second output buffer from the first power supply or the second power supply, as defined by the claimed invention. The control circuit of the present invention control to isolate the differential amplifier circuit or the second circuit (or the first circuit or the second circuit) from the first power supply or the second power supply to reduce power consumption. Thus, Applicant submits that Roe fails to show or suggest each and every element of the independent claims of the present invention. Applicant also submits that none of the cited prior art (D'Souza, Aoki, Oldham) make up for the above-described deficiencies of Roe and that there is no motivation to combine the references. Accordingly, Applicant requests that the rejections be withdrawn and that new claims 19-42 be allowed.

In view of the above remarks, the Applicant respectfully submits that each of claims 19-42 recite subject matter which is neither disclosed nor suggested in the cited prior art. Applicant submits that this subject matter is more than sufficient to render the claimed invention unobvious to a person of ordinary skill in the art. Applicant therefore requests that each of the claims be found allowable, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

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In the event this paper is not timely filed, the Applicants respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account No. 01-2300.

Respectfully submitted,

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Attachments Marked-up copy of the amended paragraphs of the specification
Request for Approval of Drawing Corrections
Corrected Drawing Figure 6

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MARKED-UP COPY OF AMENDMENTS TO SPECIFICATION

Please replace page 14, paragraph 2 with:

When the integrated circuit device 21 is mounted on a printed circuit board, the input buffer circuit 1 receives the input signal IN having a full amplitude. Accordingly, the transfer circuit 4A is used in the normal usage. The input buffer circuit 1 receives an input control signal St high via a pad P2. As a result, a control signal /St low is supplied to the gates of the NMOS transistors Tn4 and Tn5 and the PMOS transistors Tp3-Tp5 of Fig. 2. The transfer circuit 4A is enabled and the input operation for the full-amplitude input signal IN is carried out with low power consumption.

Switch SW1 is closed while switch SW2 is open.

Please replace page 15, paragraph 4 (lines 1-6) with:

That is, in operational test mode, the proper operational test on the output buffer circuit 23 is performed by enabling the differential amplifier circuit 2. When a user uses the input/output buffer circuit 22, on the other hand, the consumed power of the input buffer circuit 1 is reduced by enabling the transfer circuit 4A. In the case

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